

IKSHITH ITTY JIBU

Electronic Design Engineer | Embedded Systems | Wearable and Low-Power Hardware
ikshithittyjibu@gmail.com | +44 7340 766893 | [linkedin.com/in/ikshithij](https://www.linkedin.com/in/ikshithij) | [ikshith.com](https://www.ikshith.com) | London, UK

PROFILE

Electronic design engineer who takes hardware from architecture to working product: system specification, schematic capture, multilayer PCB layout, firmware bring-up, and design-for-manufacture. I lead electronics for three product verticals and define system architecture for two more at Morph, a stealth-stage wearable technology startup building soft-robotic and pneumatic systems, a domain with few off-the-shelf references. To date I have designed more than 25 distinct PCBs across the product range, from 17 mm 4-layer modules to boards over 180 mm, with over 100 units now in use for investor demos, internal data capture, and validation. MSc Analogue and Digital IC Design, Imperial College London; BEng First Class, University of Surrey.

EXPERIENCE

Electronic Design Engineer

Oct 2024 to Present

Morph (formerly Botz Innovation), Wearable Technology, Soft Robotics and Pneumatics, London

- **Lead electronics design across three product verticals** independently, from system spec through schematic, multilayer PCB layout, prototyping and iterative debug, spanning low-power 3.3 V logic, sensing front-ends, and higher-current pneumatic drive.
- **Designed more than 25 distinct PCBs** ranging from 17 mm 4-layer modules to boards over 180 by 80 mm; over 100 units built (in-house assembly following CM coordination) and reliably running across multiple hardware iterations.
- **Own system architecture for two further verticals**, selecting components, defining wiring topology and interfaces, and specifying intended behaviour at the block level.
- **Designed power architecture across the product range**, buck, boost and LDO regulation tuned for efficiency on packs from a 100 mAh LiPo up to an 18650 (Samsung 30Q, 3000 mAh, 15 A continuous discharge).
- **Designed a coplanar waveguide feed for a chip antenna on an nRF5340**, with impedance matching and trace geometry calculated in AppCAD.
- **Review electronics and PCB designs for a graduate engineer**, providing technical direction across layout and bring-up.
- **Bring up custom boards independently**, device-tree configuration, validation firmware and bring-up scripts to confirm peripheral and power behaviour; working knowledge of Zephyr RTOS and the supporting toolchain.
- **Coordinate directly with contract manufacturers and suppliers**, RFQs, DFM review, BOM cost and first-article builds, and assemble pneumatic subsystems hands-on, informing electronics packaging.

Electronic and Embedded Software Engineer

Jun 2023 to Sept 2023

CDO2, Sussex Innovation Centre, Innovate UK Programme

- **Led PCB design and production** for custom Atmel SAM 32-bit MCU development boards, the core of a battery current-density analyser using classical and quantum sensors.
- **Delivered hardware for quantum sensor integration** in collaboration with the University of Sussex Quantum Systems and Devices team.
- **Designed a Mu-metal shielding chassis** that reduced electromagnetic interference in sensitive current measurements; deployed embedded firmware via ASF and Docker. Mentored two interns and one A-level student.

Student Ambassador

2019 to 2022

University of Surrey, Electrical and Electronic Engineering

- Designed and led PCB soldering workshops for over 200 prospective students (featured in departmental media); ran placement-year Q&A sessions for incoming students and parents.

EDUCATION

MSc Analogue and Digital Integrated Circuit Design, Merit

Sept 2023 to Sept 2024

Imperial College London

Full-Custom IC Design (Cadence Virtuoso), Analogue Signal Processing, Sensors and Instrumentation, Biomedical Electronics, High-Performance Electronic Systems

BEng Electrical and Electronic Engineering, First Class Honours

Sept 2018 to Jun 2022

University of Surrey

Power Electronics, DSP, Control Engineering, Nanotechnology, Photonics, C++, Computer Architecture. Highest mathematics average in cohort (95%).

SELECTED PROJECTS

Much of my current work at Morph is under NDA. The projects below are ones I can discuss freely and that demonstrate my hardware, analogue and IC design depth.

- **10-bit R-2R DAC, 90 nm CMOS (Imperial):** full-custom integrated circuit in Cadence Virtuoso, exceeding the 8-bit project specification. Designed the R-2R ladder, shift registers, ring oscillator and voltage reference; performed stability and noise analysis, device characterisation, and the digital backend flow (RTL, synthesis, place and route).
 - **Graphene CMOS ISFET breath analysis (Imperial, A+, top of cohort):** feasibility study for non-invasive respiratory disease screening. Cleanroom transfer of graphene onto an ISFET sensing array, a breath-condensate collection and test system built to run in under 10 minutes, and a reproducible MATLAB analysis pipeline still in use.
 - **Vector Impedance Meter (Imperial, A, one of the best in cohort):** STM32F405-based instrument measuring complex impedance from 100 Hz to 100 kHz at over 90% accuracy. Op-amp analogue front-end, LTspice simulation, custom PCB, GC9A01 display, Kelvin clips and a 3D-printed enclosure.
 - **Hotspot Detection in Photovoltaic Modules (Surrey, self-proposed):** smart embedded system with an analogue switching circuit that disconnects faulty solar cells to protect module performance. 100% in-spec fault detection, mathematical fault models, and JSON telemetry over a LoRa network.
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TECHNICAL SKILLS

Hardware	Schematic capture, multilayer PCB layout, RF including CPW and chip-antenna feeds, power architecture (buck, boost, LDO), DFM, BOM, CM coordination
EDA and Sim	KiCad, Cadence Virtuoso, LTspice, FreeCAD, AppCAD
Embedded	nRF5340, nRF52840, STM32, Atmel SAM, ESP32, Zephyr RTOS, Bluefruit BLE, device tree, board bring-up
Protocols	BLE (GATT and HID), UART, SPI, I2C, LoRa, USB CDC
Software	VS Code, Cursor, nRF Connect SDK, Arduino CLI, Git, Docker, PlatformIO, ESP-IDF
IC Design	Full-custom CMOS (90 nm and 0.35 μ m), RTL, synthesis, place and route, MATLAB
Fabrication	BGA and 0201 hand placement, wedge wire bonding, cleanroom assembly, 3D printing, laser cutting, pneumatic assembly
Languages	Native English and Hindi, fluent Malayalam

RECOGNITION AND MEDIA

- Consistent First Class distinctions across university project portfolio (undergraduate and postgraduate); highest mathematics average at Surrey (95%); Mentor's Honour Award (A-Level), top of cohort.
 - Featured in University of Surrey departmental media: [Placement Year video](#) and [On the Couch interview](#).
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References on request ikshith.com Updated May 2026